Remarks

The Examiner is thanked for granting a telephonic interview with the Applicants' representative on March 28, 2006. Claims 1, 2, 6-11, 13-15, 18, and 19 are currently pending in the present application. The Applicants have amended Claims 1, 2, 6, 8, and 9 in accordance with the March 28, 2006 interview. In view of the foregoing amendments and following remarks, reconsideration and withdrawal of the 35 U.S.C. §103 grounds of rejection is respectfully requested.

Claim Rejections Under 35 U.S.C. §103

Claims 1, 2, 6-11, 13-15, 18, and 19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,720,850 to Sasabata et al., hereinafter "Sasabata", in view of U.S. Patent No. 6,518,823 to Kawai, hereinafter "Kawai". For the reasons set forth below, reconsideration and withdrawal of this ground of rejection is respectfully requested.

Claim 1 as amended recites:

> An integrated circuit switch comprising: at least two signal ports coupled by a signal path, the signal path including a channel of at least one series FET; a shunt path coupled to ground and including a channel of a shunt FET; a first control voltage applied to the signal path; and, a second control voltage applied to a gate of the series FET and to a drain/source of the shunt FET, wherein a drain terminal of the shunt FET is directly and *continuously* coupled to a gate terminal of the series FET. [emphasis added.]

As indicated above, Claim 1 recites a switching device comprising at least one series FET and a shunt FET. (see Figure 3 of the specification). As explained in the September 14, 2005 Response to the June 28, 2005 Office Action, important to the claimed configuration is the drain terminal of the shunt FET being directly coupled to the gate of the series FET. (see September 14, 2005 response, fourth paragraph under the heading "Remarks"). In the instant Response, the term "continuously" has been added to Claim 1 solely to better describe the direct coupling relationship

between the drain terminal of the shunt FET and the gate of the series FET, as previously explained in the September 14, 2005 Response. Accordingly, since this relationship has already been searched and examined, the Applicants respectfully request that this amendment be entered.

As noted in the prior Response, direct *(and continuous)* coupling between the drain terminal of a shunt FET and the gate of a series FET enables a single control signal to have the opposite effect on each transistor (i.e., turning one ON when the other is OFF, and vice versa), and to thus permit a common logic signal to control both transistors (see page 7, paragraphs [0029]-[0030] of the specification). Indeed, if the direct and continuous coupling feature recited in Claim 1 were replaced with say, a switching function, a single control signal would not be able to both turn one transistor ON while turning another transistor OFF, and vice versa. (emphasis added).

The Applicants now address the Sasabata and Kawai references cited in the present Office Action. Sasabata relates to a single-pole double-throw (SPDT) switch for use in providing attenuation to a high-frequency signal during conduction. In particular, Sasabata discloses a SPDT switch 41 comprising series FETs, 43, 46, a constant voltage source 50 connected to the sources of FETs 43 and 46, and a variable-voltage generator 52 connected to the gates of FETs 43 and 46. (see Figure 5 and column 9, line 40 to column 10, line 8 of Sasabata). The variable-voltage generator 52 "...switches between a voltage Vα ... and Vcc, thereby feeding the voltage Vα or Vcc to the gates of FETs 43 and 46". (emphasis added). (see column 10, lines 4-8 of Sasabata).

As indicated by the Examiner, Sasabata fails to disclose a shunt FET wherein a drain terminal of the shunt FET is directly coupled to a gate terminal of a series FET. The Examiner proposes, however, that replacing the switch within the semi-conductor circuit 52 of Sasabata with a transmission gate structure 52 taught in Kawai yields a shunt FET structure equivalent to the shunt FET as claimed.

Referring now to Kawai, Kawai discloses an integrated circuit in which a one-time programmable logic device disables writing to a storage device once a current is passed therethrough. (see Abstract of Kawai). In particular, with regards to Figures 7 and 8, Kawai discloses a semi-conductor switch 52 having a contact 52a connected to a fuse 18, a fixed contact 52b connected to output of a SUR circuit 16, a second fixed contact 52c connected to a pad 22 and external power supply 24, and a switching control terminal 52d connected to a pad 54 serving as an internal terminal for reading/writing control. (see Kawai at column 7 lines 51-64). This semi-conductor switch 52 further comprises transmission gates 61 and 62, each formed by a CMOS transistor with small power consumption and an inverter 63. (see column 8, lines 54-58 of Kawai).

As indicated above, the Examiner suggests combining the semi-conductor switch 52 taught by Kawai with the SPDT switch 41 of Sasabata. The Applicants respectfully submit, however, that even if feasible, such a combination would fail to result in the switch recited in Claim 1. As shown in Figure 5 of Sasabata, a voltage source Vcc provides voltage to a switch (i.e., the Kawai 52 switch) and to the gate of FET 43, but only if the Kawai switch 52 is in one position. If, however, an alternate voltage is desired, (i.e., the switch 52 is in its alternate position), the connection between the drain 52a of the Kawai switch (52) and the gate of the Sasabata switch 43 would be severed, thereby preventing a single control signal from having an opposite effect on the switches.

Accordingly, since the Sasabata-Kawai combination fails to disclose, teach or suggest every claim limitation of Claim 1, Applicants respectfully submit that Claim 1 is patentable over the Sasabata-Kawai combination and respectfully request reconsideration and withdrawal of this ground of rejection with respect to Claim 1.

Independent claims 2, 6, 8, and 9 include similar limitations to those discussed above with regard to Claim 1. Therefore, for at least those reasons discussed above with respect to Claim 1,

reconsideration and withdrawal of this rejection with respect to claims 2, 6-11, 13-15, 18, and 19 is also respectfully requested.

Conclusion

In view of the foregoing amendments and remarks, the Applicants submit that the present Application, including claims 1, 2, 6-11, 13-15, 18 and 19, is now in condition for allowance an indication reflecting the same is earnestly solicited. The Applicants further request that the aforementioned claim amendments be entered for the reasons indicated above.

Respectfully submitted,

Paul A. Taufer
Reg. No. 35,703
Richard L. Cruz
Reg. No. 52,783

PAT:RLC:nn

DLA Piper Rudnick Gray Cary LLP
One Liberty Place
1650 Market Street, Suite 4900
Philadelphia, PA. 19103
Phone: 215.656.3300